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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/609,813	07/03/2000	Leonard Forbes	M4065.0051/P051-A	4281

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EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/609,813	Applicant(s) FORBES ET AL.	
	Examiner Paul E Brock II	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *48-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *48-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 48 – 61 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 48 and 55 the phrase "incorporating said multi-region planar thyristor in a memory device, said memory device adapted to store information using said latchup of said multi-region planar thyristor," is a method of using and intended use limitation. It is not clear how this method of using recitation further defines the claimed invention with respect to the method of making. Therefore, "incorporating said multi-region planar thyristor in a memory device, said memory device adapted to store information using said latchup of said multi-region planar thyristor," does not further distinguish the claimed invention over the prior art.

Further claim 55 recites the limitation "said gate adapted to receive a voltage for producing latch-up in said multi-region planar thyristor" is an intended use recitation which does not further define the method of making the semiconductor device.

In claim 62 the phrase "for producing latchup in said multi-region planar thyristor, whereby said thyristor transitions from a first one to a second one of said at least two possible current states," is a method of using and intended use limitation. It is not clear how this method of using recitation further defines the claimed invention with respect to the method of making.

Therefore, "for producing latchup in said multi-region planar thyristor, whereby said thyristor transitions from a first one to a second one of said at least two possible current states," does not further distinguish the claimed invention over the prior art.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 48 – 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno (USPAT 5346838, Ueno) in view of Bhagat (USPAT 4861731).

Ueno discloses in figure 3 a method of forming a circuit for storing information as one of at least two possible stable current states in figures 3 – 6.

With regard to claim 48 and 55, Ueno discloses in figure 3 providing a semiconductor substrate (11). Ueno discloses in figure 3 providing doped silicon regions to from a multi-region planar thyristor having at least four regions. Ueno discloses in figure 3 forming at least one polysilicon gate (20) overlying a junction of the multi-region planar thyristor thereby making the junction a gated diode. Ueno discloses in figures 3 and 4 connecting the at least one polysilicon gate to a voltage source (G) for producing latch-up in the multi-region planar thyristor. Ueno discloses in figures 3 and 4 incorporating said multi-region planar thyristor in a memory device, said memory device adapted to store information using said latchup of said multi-region planar

thyristor. Ueno doe not disclose that the junction is defined only by a single junction. Bhagat teaches in figure 1 forming at least one gate (54) overlying a single junction (the junction between regions 36 and 45). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the gate overlying a single junction of Bhagat in the method of Ueno in order to turn the thyristor off as stated by Bhagat in column 6, lines 15 – 18.

With regard to claim 49 and 56, Ueno discloses in figure 3 providing doped silicon regions that form a seven region planar thyristor.

With regard to claim 50 and 57, Ueno discloses in figure 3 providing doped silicon regions that form a p-n-p-n-p-n-p planar thyristor.

With regard to claim 52 and 59, Ueno discloses in figure 4 the step of providing doped silicon regions further comprises forming two memory cells (CH0 and CH1)

With regard to claim 53 and 60, Ueno discloses in figures 3 and 4 connecting a central region of the seven-region planar thyristor to a shared row address line (C).

With regard to claim 54 and 61, Ueno discloses in figure 4 the step of providing doped silicon regions further comprises forming one memory cell (CH0).

With regard to claims 51 and 58, Ueno discloses a p-n-p-n-p-n-p planar thyristor. Ueno and Bhagat do not disclose an n-p-n-p-n-p-n planar thyristor. It is well known in the art to form semiconductor devices of reverse polarity. It would have been obvious to one of ordinary skill in the art at the time of the present invention to form an n-p-n-p-n-p-n planar thyristor in the method of Ueno and Bhagat for design choice of the manufacturer.

Claim 62 is rejected as applied to Ueno and Bhagat similar to the rejection of claims 48 and 55 above.

Response to Arguments

5. Applicant's arguments filed October 15, 2002 have been fully considered but they are not persuasive.

6. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

7. With regard to the applicant's argument that "A structure combining the features of the Bhagat and Ueno devices would be inoperative, since no back contact could be made through the Bhagat dielectric layer." It should be noted that the only feature that is relied upon in the Bhagat reference is "at lest one polysilicon gate overlying a single junction." Nothing in the rejection suggests combining the dielectric layer of Bhagat with the Ueno reference, and there is nothing in either reference which would suggest that the device would be inoperable if the "at lest one polysilicon gate overlying a single junction" of Bhagat was incorporated into the method of Ueno. Therefore, the rejection is proper.

8. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the suggestion to combine the references is clearly stated in paragraph 2, above and in the office action dated January 9, 2002.

9. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the

organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
November 22, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800